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10/647,217	08/26/2003	Yoshitaka Kayukawa	SON-2810	1901

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EXAMINER	
GANDHI, DIPAKKUMAR B	
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2117	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/647,217	KAYUKAWA ET AL.	
	Examiner	Art Unit	
	DIPAKKUMAR GANDHI	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) *1-23* is/are withdrawn from consideration.

5)☒ Claim(s) *36-44* is/are allowed.

6)☒ Claim(s) *24-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment

1. The amendment including amended claims filed on 02/25/2008 has been entered.

2. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 24 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 24 recites the limitation "said scan mode signal" in line 8. There is insufficient antecedent basis for this limitation in the claim.

5. Claims 25-30, 32-33, 35 are dependent claims on claim 24. Claims 25-30, 32-33, 35 are also rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention because of combination of additional limitations and the limitation in claim 24 mentioned above.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 31, 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashizume (US 6,539,511 B1) view of Naitoh et al. (US 5,040,150).

As per claim 31, Hashizume teaches a semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry, comprising: a plurality of flip-flops arranged so as to perform scan testing for said internal logical circuitry; memory means connected to said plurality of flip-flops and switching at a transition time between said test mode and said normal mode and for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal (fig. 1A, 1B, 2, 36, 42, "FIG. 1A schematically illustrates the overall structure of a semiconductor integrated circuit device 1 according to a first embodiment of the present invention. Referring to FIG. 1A, semiconductor integrated circuit device 1 includes pads P1 to P14 arranged along the periphery thereof, and cells C1 to C14 arranged in correspondence to pads P1 to P14 respectively. Cells C1 to C 14 each include an input/output cell (I/O cell) for inputting and/or outputting a signal from/to the respective pads P1 to P14, and a test cell including a boundary scan register provided in correspondence to the I/O cell. The boundary scan registers included in cells C1 to C14 are serially connected by a scan path 4 and can serially transfer test data. In a normal operation mode, the boundary scan registers included in cells C1 to C14 are in through-states for transferring signals between a corresponding buffer (input or output buffer) and an internal logic circuit 2. FIG. 1A shows no JTAG test Circuit, for simplifying the illustration.

The semiconductor integrated circuit device 1 shown in FIG. 1A is further provided with a DC test control circuit 3. DC test control circuit 3 sets the boundary scan registers included in cells C1 to C14 in set states or reset states, thereby setting signal input/output states of the corresponding I/O cells.

A direct current (DC) test can be performed by utilizing cells for performing a boundary scan test, without providing additional components. In general, the scan path 4 forms a serial data transfer path in the boundary scan test (JTAG test). Referring to FIG. 1A, one of pads P10 and P9 serves as a test data input terminal and the other pad P9 or P10 serves as a test data output terminal, for serially inputting/outputting test data. The boundary scan registers included in cells C1 to C14 are set in set/reset

states –through the internally provided DC test control circuit 3, whereby no dedicated circuit for setting DC test data need be arranged for each pin terminal.

FIG. 1B illustrates the structure of each cell C shown in FIG. 1A, and illustrates an input/output cell (I/O cell) IOC inputting/outputting a signal, and a test cell TC provided in correspondence to the I/O cell IOC as the cell C", col. 5, line 42 to col. 6, line 14, Hashizume.

"Boundary scan registers BSR0 to BSR3 enter through states in the normal operation mode for transferring signals between output buffer 10 and input buffer 11, and internal logic circuit 2. In a boundary scan test operation mode, boundary scan registers BSR0 to BSR3 form a serial scan path for serially transferring test data", col. 6, lines 46-51, Hashizume.

"FIG. 2 illustrates an exemplary structure of each boundary scan register BSR shown in FIG. 1B. Referring to FIG. 2, boundary scan register BSR includes a multiplexer (MUX) 20 selecting one of a shift-in data signal SI and an internal data signal DI in accordance with a shift mode instruction signal SFMD, a flip-flop (shift register) 21 capturing and transferring a signal supplied from multiplexer 20 in accordance with a shift clock signal SHIFT, a through latch 22 capturing the output signal of flip-flop 21 in accordance with an update instruction signal UPDATE, and a multiplexer (MUX) 23 selecting and outputting one of internal data signal DI and an output signal of through latch 22 in accordance with a mode instruction signal MODE", col. 7, lines 13-25, Hashizume.

"FIG. 36 illustrates the structure of a main part of a semiconductor integrated circuit device according to a seventeenth embodiment of the present invention. In the structure shown in FIG. 36, two test modes EXTEST1 and EXTEST2 are prepared for a boundary scan test circuit. When an external test instruction EXTEST1 or EXTEST2 is set in an instruction register 41, an instruction decoder 42 supplies a DC test mode control signal DCTM setting all boundary scan registers provided in correspondence to output cells included in a boundary scan register chain (BSR chain) 100 to set or reset states to a BSR control circuit 30 (or 3). BSR control circuit 30 (or 3) drives a set signal Set or a reset signal Reset to an active state in accordance with DC test mode control signal DCTM supplied from instruction decoder 42 and sets the boundary scan registers corresponding to the output cells included in BSR chain 100 to set or reset states.

An external instruction EXTEST, which is generally utilized in a boundary scan test, is an instruction for performing data input/output between the boundary scan registers and a device external to the device (integrated circuit device). The external test instruction EXTEST is employed in verifying connection between the integrated circuit device (device) and an external logic circuit or testing the external logic circuit. When the external test instruction EXTEST is supplied, a cell connected to an output pin terminal of boundary scan register chain (BSR chain) 100 outputs data", col. 33, lines 49 to col. 34 line 8, Hashizume.

"When the external test instruction EXTEST1 or EXTEST2 is supplied, instruction decoder 42 supplies a DC test mode control signal DCTM to BSR control circuit 30 (or 3) for setting the boundary scan registers included in BSR chain 100 in set or reset states. Therefore, no time is required for preloading and a shift operation dissimilarly to an ordinary boundary scan test, and the output cell (including an I/O cell) is simply set in a set or reset state, and signals of "1" or "0" can be output from all output terminals by setting the boundary scan registers connected to the output terminals and an output control signal to set/reset states. Thus, the voltage levels of the output signals can be readily measured", col. 34, lines 31-43, Hashizume. "FIG. 42 shows flip-flops (FF) 21-0 and 21-1 included in output boundary scan registers (boundary scan registers connected to output buffers) BSR0", col. 37, lines 39-42, Hashizume).

However Hashizume does not explicitly teach the specific use of access control means for prohibiting access to said memory means during said test mode in accordance with a mode signal, whereby said prohibiting is always performed during said test mode.

Naitoh et al. in an analogous art teach that by making "L" the test mode signal TM supplied from the outside, the built-in RAM 203 is disconnected from the random logic circuit 202, and the common test terminals are set to a test state (col. 15, lines 1-4, Naitoh et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hashizume's patent with the teachings of Naitoh et al. by including an additional step of using access control means for prohibiting access to said memory means during said test mode in accordance with a mode signal, whereby said prohibiting is always performed during said test mode.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to control access to the memory during the test mode.

- As per claim 34, Hashizume and Naitoh et al. teach the additional limitations.

Hashizume teaches a method of testing a semiconductor integrated circuit, which has internal logical circuitry, a plurality of flip-flops for scan testing said internal logical circuitry and memory means connected to said plurality of flip-flops, which has a normal operation mode and a test mode for performing said scan testing (fig. 1A, 1 B, 2, 42, "FIG. 1A schematically illustrates the overall structure of a semiconductor integrated circuit device 1 according to a first embodiment of the present invention. Referring to FIG. 1A, semiconductor integrated circuit device 1 includes pads P1 to P14 arranged along the periphery thereof, and cells C1 to C14 arranged in correspondence to pads P1 to P14 respectively. Cells C1 to C 14 each include an input/output cell (I/O cell) for inputting and/or outputting a signal from/to the respective pads P1 to P14, and a test cell including a boundary scan register provided in correspondence to the I/O cell. The boundary scan registers included in cells C1 to C14 are serially connected by a scan path 4 and can serially transfer test data. In a normal operation mode, the boundary scan registers included in cells C1 to C14 are in through-states for transferring signals between a corresponding buffer (input or output buffer) and an internal logic circuit 2. FIG. 1A shows no JTAG test Circuit, for simplifying the illustration.

The semiconductor integrated circuit device 1 shown in FIG. 1A is further provided with a DC test control circuit 3. DC test control circuit 3 sets the boundary scan registers included in cells C1 to C14 in set states or reset states, thereby setting signal input/output states of the corresponding I/O cells.

A direct current (DC) test can be performed by utilizing cells for performing a boundary scan test, without providing additional components. In general, the scan path 4 forms a serial data transfer path in the boundary scan test (JTAG test). Referring to FIG. 1A, one of pads P10 and P9 serves as a test data input terminal and the other pad P9 or P10 serves as a test data output terminal, for serially inputting/outputting test data. The boundary scan registers included in cells C1 to C14 are set in set/reset

states –through the internally provided DC test control circuit 3, whereby no dedicated circuit for setting DC test data need be arranged for each pin terminal.

FIG. 1B illustrates the structure of each cell C shown in FIG. 1A, and illustrates an input/output cell (I/O cell) IOC inputting/outputting a signal, and a test cell TC provided in correspondence to the I/O cell IOC as the cell C", col. 5, line 42 to col. 6, line 14, Hashizume.

"Boundary scan registers BSR0 to BSR3 enter through states in the normal operation mode for transferring signals between output buffer 10 and input buffer 11, and internal logic circuit 2. In a boundary scan test operation mode, boundary scan registers BSR0 to BSR3 form a serial scan path for serially transferring test data", col. 6, lines 46-51, Hashizume.

"FIG. 2 illustrates an exemplary structure of each boundary scan register BSR shown in FIG. 1B. Referring to FIG. 2, boundary scan register BSR includes a multiplexer (MUX) 20 selecting one of a shift-in data signal SI and an internal data signal DI in accordance with a shift mode instruction signal SFMD, a flip-flop (shift register) 21 capturing and transferring a signal supplied from multiplexer 20 in accordance with a shift clock signal SHIFT, a through latch 22 capturing the output signal of flip-flop 21 in accordance with an update instruction signal UPDATE, and a multiplexer (MUX) 23 selecting and outputting one of internal data signal DI and an output signal of through latch 22 in accordance with a mode instruction signal MODE", col. 7, lines 13-25, Hashizume. "FIG. 42 shows flip-flops (FF) 21-0 and 21-1 included in output boundary scan registers (boundary scan registers connected to output buffers) BSR0", col. 37, lines 39-42, Hashizume).

Naitoh et al. teach that access to said memory means is prohibited during said test mode, whereby said prohibiting is always performed during said test mode ("By making "L" the test mode signal TM supplied from the outside, the built-in RAM 203 is disconnected from the random logic circuit 202, and the common test terminals are set to a test state", col. 15, lines 1-4, Naitoh et al.).

Allowable Subject Matter

9. Claims 36-44 are allowed.

10. The following is an examiner's statement of reasons for allowance:

The present invention relates to a semiconductor integrated circuit, such as an LSI, and relates particularly to a semiconductor integrated circuit in which a scan circuit is provided, as well as a method of testing same.

The claimed invention in claim 36 recites features such as:"…a reset means for resetting said plurality of flip-flops at a transition time, between said test mode and said normal mode, responsive to said scan mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal, wherein said reset means is responsive to a reset signal inputted from a reset input terminal and resets said plurality of flip-flops at said transition time, between said test mode and said normal mode, in accordance with said mode signal."

The prior art of record (Hashizume, US 6,539,511 B1) teaches that in a semiconductor integrated circuit device supporting a boundary scan test, the state of an I/O cell is set under the control of a DC test control circuit through a boundary scan register utilized for the boundary scan test for setting an external terminal connected with a pad in a desired state (abstract, Hashizume).

Naitoh et al. (US 5,040,150) teach a semiconductor integrated circuit device comprising a first circuit forming a random logic and outputting a plurality of first parallel data of plural bits, a second circuit which receives the plurality of first parallel data and supplies a plurality of second parallel data of plural bits to the first circuit, and a test circuit which divides a part of external parallel data of plural bits smaller in number than the first parallel data into a plurality of third parallel data of plural bits in such a manner that the plurality of third parallel data correspond in number to the plurality of first parallel data (abstract, Naitoh et al.).

Cavaliere et al. (US 3,961,254) teach an LSI semiconductor device includes a memory array incorporating address, data and buffer registers, and associated combinatorial and/or sequential logic circuitry. The array is "embedded" in the sense that the memory array is not directly accessible, either in whole or in part, from the input and output terminals or pads of the device. To facilitate testing, means which bypass the associated logic circuitry are provided for scanning information directly into the address and data registers. The information so introduced is shifted through the register strings. The interconnections from the associated logic circuitry are inhibited during the testing mode while the

information shifting means are inhibited during an operative mode. The information scanned into the registers may be scanned out to determine whether there is a defect or problem in the register strings. Output levels from the array are compared with an expected output (abstract, Cavaliere et al.).

Tamamura et al. (US 6,118,316) teach a semiconductor integrated circuit generating a stabilized oscillation signal based on an input signal includes a plurality of unit circuits connected in series, each of the unit circuits having at least an oscillator, a divider, and a phase comparator which construct at least one part of a phase-locked loop. In the unit circuit, a frequency of an oscillation output signal of a latter one of the unit circuits is higher than that of an oscillation output signal of a former one of the unit circuits (abstract, Tamamura et al.).

Bae et al. (KR 2001011641 A) teach that an internal clock generating apparatus is provided to reduce test time by generating internal test clock pulses synchronized with both the rising and falling edges of a source clock signal, respectively (abstract, Bae et al.).

DeLisle et al. (US 5,283,889) teach that a relatively fast system control processor, such as an Intel 8051, is substituted for an Intel 8042 microprocessor in a PC/AT type compatible personal computer. In one embodiment of the invention, a System Control Processor Interface (SCPI) is provided between the central processing unit (CPU) and the system control processor (SCP) to maintain compatibility with the PC/AT bus. The combination of the faster SCP and the SCPI interface improves the overall system performance. Control circuitry is also provided for setting the A20 signal relatively quickly to allow memory access above one megabyte (abstract, DeLisle et al.).

Yutaka (JP 63134970) teaches that design data of an IC 10 consisting of a logic circuit group before inserting a scan latch is read from a fundamental data holding part 11, and the confirmation facility of existence of a fault in an input end and an output end of a circuit is calculated by a fault existence confirmation facility calculating part 12. Also, by a control facility calculating part 13, the setting facility of a signal to the input end for confirming a fault is calculated. Subsequently, their rank order is discriminated by rank order discriminating parts 14, 15, and in order from that which is inferior inconfirmation facility, and that which is inferior in control facility, a write/read scanning circuit is inserted,

and FFs 1 W8 become scan FFs. In this state, a regular scan test and a non-scan test are executed (abstract, Yutaka).

Ichiro (JP 04287510) teaches a usual flip-flop 17 acts like a usual flip-flop when an MD is zero and a scanning flip-flop 18 reaches the data load state. When the MD is '1', the scanning flip-flop 18 acts like a usual flip-flop and the usual flip-flop 17 reaches the data load state, then each clock is made independent. The test of the circuit by scanning is executed independently of the kind and state of a system clock signal (abstract, Ichiro).

The prior arts however do not teach a reset means for resetting said plurality of flip-flops at a transition time, between said test mode and said normal mode, responsive to said scan mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal, wherein said reset means is responsive to a reset signal inputted from a reset input terminal and resets said plurality of flip-flops at said transition time, between said test mode and said normal mode, in accordance with said mode signal.

Hence the prior arts of record do not anticipate nor render obvious the claimed invention. Thus, claim 36 is allowable over the prior arts of record. Claims 37-40 are allowed because of the combination of additional limitations and the limitations listed above.

- The claimed invention in claim 41 recites features such as:"…a reset input signal for controlling reset of said flip-flops by a reset control block provided to detect a transition time of a logical level of the scan mode signal by an edge detection signal having a pulse length that is at least equal to or greater than one clock period of a system clock, wherein scan operations are inhibited without resetting at the time of initiating scan operations or normal operations without being reset upon termination of scan operations, whereby said resetting is always performed at said transition time."

The prior art of record (Hashizume, US 6,539,511 B1) teaches that in a semiconductor integrated circuit device supporting a boundary scan test, the state of an I/O cell is set under the control of a DC test control circuit through a boundary scan register utilized for the boundary scan test for setting an external terminal connected with a pad in a desired state (abstract, Hashizume).

Naitoh et al. (US 5,040,150) teach a semiconductor integrated circuit device comprising a first circuit forming a random logic and outputting a plurality of first parallel data of plural bits, a second circuit which receives the plurality of first parallel data and supplies a plurality of second parallel data of plural bits to the first circuit, and a test circuit which divides a part of external parallel data of plural bits smaller in number than the first parallel data into a plurality of third parallel data of plural bits in such a manner that the plurality of third parallel data correspond in number to the plurality of first parallel data (abstract, Naitoh et al.).

Cavaliere et al. (US 3,961,254) teach an LSI semiconductor device includes a memory array incorporating address, data and buffer registers, and associated combinatorial and/or sequential logic circuitry. The array is "embedded" in the sense that the memory array is not directly accessible, either in whole or in part, from the input and output terminals or pads of the device. To facilitate testing, means which bypass the associated logic circuitry are provided for scanning information directly into the address and data registers. The information so introduced is shifted through the register strings. The interconnections from the associated logic circuitry are inhibited during the testing mode while the information shifting means are inhibited during an operative mode. The information scanned into the registers may be scanned out to determine whether there is a defect or problem in the register strings. Output levels from the array are compared with an expected output (abstract, Cavaliere et al.).

Tamamura et al. (US 6,118,316) teach a semiconductor integrated circuit generating a stabilized oscillation signal based on an input signal includes a plurality of unit circuits connected in series, each of the unit circuits having at least an oscillator, a divider, and a phase comparator which construct at least one part of a phase-locked loop. In the unit circuit, a frequency of an oscillation output signal of a latter one of the unit circuits is higher than that of an oscillation output signal of a former one of the unit circuits (abstract, Tamamura et al.).

Bae et al. (KR 2001011641 A) teach that an internal clock generating apparatus is provided to reduce test time by generating internal test clock pulses synchronized with both the rising and falling edges of a source clock signal, respectively (abstract, Bae et al.).

DeLisle et al. (US 5,283,889) teach that a relatively fast system control processor, such as an Intel 8051, is substituted for an Intel 8042 microprocessor in a PC/AT type compatible personal computer. In one embodiment of the invention, a System Control Processor Interface (SCPI) is provided between the central processing unit (CPU) and the system control processor (SCP) to maintain compatibility with the PC/AT bus. The combination of the faster SCP and the SCPI interface improves the overall system performance. Control circuitry is also provided for setting the A20 signal relatively quickly to allow memory access above one megabyte (abstract, DeLisle et al.).

Yutaka (JP 63134970) teaches that design data of an IC 10 consisting of a logic circuit group before inserting a scan latch is read from a fundamental data holding part 11, and the confirmation facility of existence of a fault in an input end and an output end of a circuit is calculated by a fault existence confirmation facility calculating part 12. Also, by a control facility calculating part 13, the setting facility of a signal to the input end for confirming a fault is calculated. Subsequently, their rank order is discriminated by rank order discriminating parts 14, 15, and in order from that which is inferior inconfirmation facility, and that which is inferior in control facility, a write/read scanning circuit is inserted, and FFs 1 W8 become scan FFs. In this state, a regular scan test and a non-scan test are executed (abstract, Yutaka).

Ichiro (JP 04287510) teaches a usual flip-flop 17 acts like a usual flip-flop when an MD is zero and a scanning flip-flop 18 reaches the data load state. When the MD is '1', the scanning flip-flop 18 acts like a usual flip-flop and the usual flip-flop 17 reaches the data load state, then each clock is made independent. The test of the circuit by scanning is executed independently of the kind and state of a system clock signal (abstract, Ichiro).

The prior arts however do not teach a reset input signal for controlling reset of said flip-flops by a reset control block provided to detect a transition time of a logical level of the scan mode signal by an edge detection signal having a pulse length that is at least equal to or greater than one clock period of a system clock, wherein scan operations are inhibited without resetting at the time of initiating scan operations or normal operations without being reset upon termination of scan operations, whereby said resetting is always performed at said transition time.

Hence the prior arts of record do not anticipate nor render obvious the claimed invention. Thus, claim 41 is allowable over the prior arts of record. Claims 42-44 are allowed because of the combination of additional limitations and the limitations listed above.

- Thus, claims 36-44 are allowable over the prior arts of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DIPAKKUMAR GANDHI whose telephone number is (571)272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JACQUES H LOUIS-JACQUES/
Supervisory Patent Examiner, Art Unit 2117

/Dipakkumar Gandhi/
Examiner, Art Unit 2117